WHAT IS CLAIMED IS:

1. A circuit apparatus operable under a specified operation voltage, the circuit apparatus comprising:

a first transistor having a first breakdown voltage and operating under a first operation voltage;

a second transistor having a second breakdown voltage and operating under a second operation voltage; and

an interface unit serially coupled to the first transistor and the second transistor for preventing the first operation voltage higher than the first breakdown voltage and the second operation voltage higher than the second breakdown voltage;

wherein the specified operation voltage is higher than both the first operation voltage and the second operation voltage.

2. The circuit apparatus according to claim 1, wherein the interface unit comprises:

a resistor; and

a capacitor connected to the resistor in parallel.

3. The circuit apparatus according to claim 1, wherein the interface unit is a third transistor having a third breakdown voltage higher than the first breakdown voltage.

4. The circuit apparatus according to claim 3, wherein the third transistor has a gate for receiving a first control signal.

5. The circuit apparatus according to claim 3, wherein the third transistor is an NMOS transistor.

6. The circuit apparatus according to claim 3, wherein the third transistor is a PMOS transistor.

7. The circuit apparatus according to claim 3, wherein the third transistor is

a CMOS transistor.

8. The circuit apparatus according to claim 3, wherein the third transistor operates in a triode region or a saturation region.

9. The circuit apparatus according to claim 1, wherein an avalanche breakdown is caused when the first transistor is operating under the specified operation voltage.

10. A circuit apparatus operable under a specified operation voltage, the circuit apparatus comprising:

a first transistor having a first breakdown voltage and operating under a first operation voltage; and

an interface unit coupled to the first transistor for preventing the first operation voltage higher than the first breakdown voltage;

wherein the specified operation voltage is higher than the first breakdown voltage.

11. The circuit apparatus according to claim 10, wherein the first transistor is a PMOS transistor.

12. The circuit apparatus according to claim 10, wherein the first transistor is an NMOS transistor.

13. The circuit apparatus according to claim 10, wherein the interface unit comprises:

a resistor; and

a capacitor connected to the resistor in parallel.

14. The circuit apparatus according to claim 10, wherein the interface unit is a second transistor.

15. The circuit apparatus according to claim 14, wherein the second transistor has a second breakdown voltage higher than the first breakdown voltage.

16. The circuit apparatus according to claim 14, wherein the second transistor has a gate for receiving a first control signal to make the circuit apparatus in a power-saving mode.

17. The circuit apparatus according to claim 14, wherein the second transistor is an NMOS transistor.

18. The circuit apparatus according to claim 14, wherein the second transistor is a PMOS transistor.

19. The circuit apparatus according to claim 14, wherein the second transistor is a CMOS transistor.

20. The circuit apparatus according to claim 14, wherein the second transistor operates in a triode region or a saturation region.